IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s)	:	Kenneth Shepard			
Serial No.	:	09/591,270	Examiner	:	Ayal I. Sharon
Filed	:	June 9, 2000	Art Unit	:	2123
For	:	METHODS FOR ESTIMATING THE BODY VOLTAGE OF DIGITAL PARTIALLY DEPLETED SILICON-ON-INSULATOR CIRCUITS			

SUPPLEMENTAL DECLARATION PURSUANT TO 37 C.F.R. § 1.131

I hereby certify that this paper is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Arlington, VA 22313-1450

January 31, 2005
Date of Deposit

Paul Ackerman
Attorney Name

39,891
PTO Registration No

Signature

1/31/05
Date of Signature

Commissioner for Patents
P.O. Box 1450
Arlington, VA 22313-1450

Dear Sir:

I, Kenneth L. Shepard, hereby declare as follows:

1. I am the inventor of the inventions as recited in claims 1-8 and 12-22 of the above-identified patent application, which are directed to methods for estimating the body voltage of digital partially depleted silicon-on-insulator circuits;
2. This Declaration Pursuant to 37 C.F.R. § 1.131 supplements my Section 1.131 declaration dated November 15, 2003;
3. Independent claim 1, from which all of claims 2-8 and 11-15 depend, is directed to "[a] method for statically estimating a body voltage of one or more transistors which form digital partially depleted silicon-on-insulator circuit having a predetermined circuit topology comprising said one or more transistors and one or more nets connecting said transistors" and comprises the following steps:

a. obtaining one or more device models, each corresponding to one of said one or more transistors;

b. abstracting each of said device models to generate one or more simplified electrical descriptions, each corresponding to one of said one or more transistors;

c. checking said predetermined circuit topology to generate one or more sets of accessible states, each set corresponding to one of said one or more transistors and being indicative of whether under any allowable switching activity, the source, gate or drain could be high or low.

d. determining one or more sets of reference state body voltage minima and reference state body voltage maxima, one for each of said one or more transistors, based on corresponding simplified electrical descriptions and corresponding sets of accessible states; and

e. ascertaining one or more target state body voltage minima and target state

body voltage maxima, one for each of said one or more transistors, based on said determined sets of reference state body voltage minima and reference state body voltage maxima;

4. Independent claim 16, from which all of claims 17-22 depend, is directed to "[a] method for analyzing an electrical property of a digital partially depleted silicon-on-insulator circuit having a predetermined circuit topology comprising one or more transistors and one or more nets," and comprises the following steps:

   a. ascertaining a target state body voltage minimum and a target state body voltage minimum for each of said transistors in said circuit;

   b. establishing an initial condition for said circuit by selecting either said target state body voltage minimum or said target state body voltage minimum for each of said transistors in said circuit;

   c. applying a voltage to said circuit; and

   d. measuring said electrical property of said circuit;

5. The inventions of claims 1-8 and 12-22 of the above-identified patent application, were actually reduced to practice in this country, prior to April 19, 1999, the filing date of Chuang et al., U.S. Patent Application Publication No. US2003/0078763 A1;

6. On April 9, 1999, I made an original submission of the inventions to the International Conference on Computer-Aided Design (ICCAD). A copy of the submission was attached as Exhibit A to my November 15, 2003, declaration;

7. The as-submitted ICCAD 99 paper contained results obtained from computer code running the inventions recited in claims 1 and 16--Figures 5(a) and (b) show steady-state delays for rising and falling transitions, measured in picoseconds, for each stage

in a 15-stage inverter chain with a switching probability at the input set at 0.5 and 0.9, respectively, and Figures 6(a) and 6(b) show steady state delays for the carry chain of an eight-bit ripple carry adder using a full-adder implementation--constituting proof of actual reduction to practice of the inventions of claims 1 and 16 prior to April 9, 1999.

8. Prior to April 19, 1999, I made a presentation of the inventions. A copy of the presentation was attached as Exhibit B to my November 15, 2003, declaration;

9. The copy of the pre-April 19, 1999, presentation contained results obtained from computer code implementing the inventions recited in claims 1 and 16-- results obtained for a 16-stage static ripple-carry adder are given under the heading "preliminary timing results"--constituting proof of actual reduction to practice and due diligence of the inventions of claims 1 and 16 prior to April 19, 1999.

10. The inventions of the present application were conceived solely by me when I derived the inventive methods to which the current claims are directed. However, after I had conceived the necessary inventive methods, I directed my graduate student, Dae-Jin Kim, to implement these methods into computer code. Since Mr. Kim's implementation of the inventive methods into computer code required only ordinary skill, Mr. Kim was not identified as a co-inventor on the above-captioned patent application. I do not believe that Mr. Kim made a contribution to the conception of the invention defined by any of the current claims.

11. Notwithstanding Mr. Kim's lack of any inventive contribution to the present application, because I included results obtained from computer code written by him in

my pre-April 19, 1999, presentation, I listed Mr. Kim as a second author, as is the academic custom;

12. In addition to writing computer code under my direction, Mr. Kim was further involved in the editing and drafting of the as-submitted ICCAD 99 paper (Exhibit A, November 15, 2003, Declaration Pursuant to Section 1.131), the version that was later published in the ICCAD 99 proceedings (Exhibit 1, June 24, 2004, Response to Requirement to Submit Information Under Section 1.105), and a paper published in June 2000 in the proceedings of the 37th Conference on Design Automation (*See* February 24, 2004, Requirement to Submit Information Under Section 1.105). As a consequence of writing the computer code that was used to generate results included in each of these papers, together with his role in drafting and editing the papers, Mr. Kim is properly identified as a second author, notwithstanding his lack of an inventive role in the present application.

13. I declare further that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful statements may jeopardize the validity of the application or any patent issuing therefrom.

Date: 1/26/2005

Kenneth L. Shepard

KENNETH L. SHEPARD